

Single CuO_x Nanowire Memristor: Forming-Free Resistive Switching Behavior

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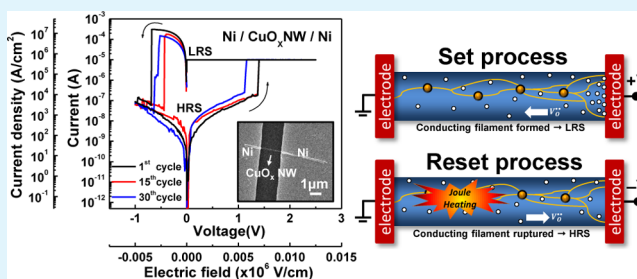
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Supporting Information

ABSTRACT: CuO_x nanowires were synthesized by a low-cost and large-scale electrochemical process with AAO membranes at room temperature and its resistive switching has been demonstrated. The switching characteristic exhibits forming-free and low electric-field switching operation due to coexistence of significant amount of defects and Cu nanocrystals in the partially oxidized nanowires. The detailed resistive switching characteristics of CuO_x nanowire systems have been investigated and possible switching mechanisms are systematically proposed based on the microstructural and chemical analysis via transmission electron microscopy.

KEYWORDS: CuO_x nanowire, ReRAM, AAO membrane, resistive switching, forming free, memristor



1. INTRODUCTION

Resistive switching random access memory (ReRAM) based on electrical resistance switches, so-called memristors, is one of the most promising candidates for next generation nonvolatile memory due to its high stacking density, low power consumption, high scalability, fast fabrication process, and multistate behaviors.^{1–4} The resistive switching phenomena in transition metal oxides, such as NiO,⁵ TiO₂,⁶ ZnO,^{7,8} and Cu₂O⁹ based on two-dimensional (2D) metal–insulator–metal (MIM) thin film structures, have been demonstrated. However, the conventional lithography has encountered the physical limit when the size of the devices is scaled down to the nanoscale. To reduce the size of the devices to achieve a higher density and improve the device performance, finding the unique properties of nanostructures is a useful way to explore the unclear nanoscale resistive switching mechanisms to understand the scalability of ReRAM.^{10–14}

One-dimensional (1D) nanostructures, especially semiconductor nanowires (NWs), have drawn much attention for various nanoelectronic applications due to their unique physical and chemical behaviors, which are different from their bulk and thin film materials, in confined dimensions and large surface-to-volume ratios.¹⁵ In recent years, top-down or bottom-up approaches have been applied to synthesize various nanostructures, including nanotubes, nanowires, and nanodots for the fabrication of nanoscale devices.^{16,17} The resistive switching characteristics of nanostructure materials, such as NiO NW,^{18–20} Co₃O₄ NW,²¹ ZnO NW,^{22,23} Cu₂O NW,²⁴ Zn₂SnO₄ NW,²⁵ and gold–Ga₂O₃ NW,²⁶ have attracted great interest in ReRAM studies.

For a large area and low-cost process, the self-assembly bottom-up approach via different templates is more promising for synthesis of nanostructures than the top-down approach.²⁷ An anodic aluminum oxide membrane (AAO) is one of self-organized templates used to form various nanostructures due to its controllable pore-diameter, depth, shape, and periodic pattern, respectively.^{28,29} Fabricated nanowire arrays by electrochemical synthesis combined with an AAO membrane is a room-temperature and low-cost, large-scale process for the production of nanoscale electronic devices. In addition, Cu is a common material for interconnects in the integrated circuit (IC). A CuO_x nanowire is anticipated to have high compatibility with modern complementary metal–oxide–semiconductor (CMOS) manufacturing techniques. In this regard, we demonstrate direct synthesis of CuO_x nanowire arrays from Cu NW arrays embedded in the AAO and each single CuO_x nanowire as a memristor exhibits a forming-free behavior. The CuO_x NWs were formed by the thermal annealing of Cu nanowire arrays that were deposited in the AAO membrane by an electrochemical plating approach. The detailed resistive switching characteristics of CuO_x NW systems have been investigated. Finally, we systematically propose possible switching mechanisms on the basis of the microstructural and chemical analysis via transmission electron microscopy (TEM).

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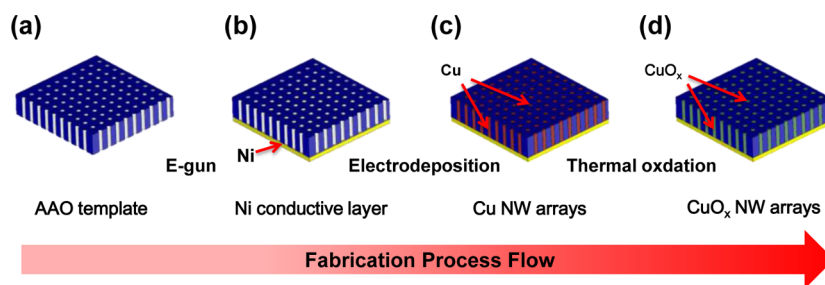


Figure 1. Schematics of the fabrication processes of CuO_x NW array. (a) Free-standing AAO with high aspect ratio nanochannels, (b) Ni conductive layer deposited by e-beam evaporation, (c) Cu NW array synthesized by pulse electrodeposition, and (d) oxidation process.

2. EXPERIMENTAL SECTION

2.1. Synthesis of AAO.³⁰ To fabricate an anodic aluminum oxide (AAO) template with a pore diameter of ~ 50 nm, a two-step anodization process was usually used. Before the anodization, high-purity Al (99.997%) sheets were sliced into 1×2 cm samples. Then, these samples were electropolished in a perchloric acid (HClO_4)/ $\text{C}_2\text{H}_5\text{OH}$ (1:4 in volume) solution for a few seconds at 10°C . In the first step, the pretreated Al samples were anodized at a constant voltage of 40 V in 0.3 M oxalic acid ($\text{H}_2\text{C}_2\text{O}_4$) solution for 30 min at 10°C . The previously formed AAO films were etched in a mixed solution of 0.2 M H_2CrO_4 and 0.4 M H_3PO_4 for 30 min at 60°C . After that, the second anodization was performed for 10 h. Besides, a current limited anodization method was utilized for thinning the barrier layer at the bottom of anodic porous alumina templates.

2.2. Electrochemical Deposition of Cu Nanowire Array from AAO Template. Anodic aluminum oxide (AAO) ~ 50 nm in diameter was used as the template for the electrochemical deposition of Cu NW arrays. To make sure the electric contact, a thin nickel (Ni) layer (about 200 nm) serving as working electrode was deposited on the one side of the AAO template by electron beam evaporation in a vacuum of $\sim 5 \times 10^{-6}$ Torr. The electrodeposition of copper nanowires was carried out in an electrolyte, containing 0.7 M $\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$ (99.5%, SHOWA) and deionized (DI) water with a pH value between 3 and 4. Electrochemical depositions were performed at room temperature (RT) using a galvanostatic pulse technique in a two-electrode electrochemical cell, having a graphite counter electrode. Magnetic stirring was applied to improve the diffusion of Cu ions at the cathode. The rotation speed was limited to avoid formation of air bubbles into the electrolyte. The Cu NWs electrodeposition process was based on modulated pulse signals in the microsecond range. During the pulse of negative current (-0.4 A, 10 ms), Cu nanowires were deposited. After the pulse deposition, a zero-bias of 50 ms was used to recover the ion concentration. The deposition process mentioned above was called a cycle. The resulting length of NWs was about 20 μm .

2.3. Formation of CuO_x Nanowire Arrays by Oxidation Process. CuO_x nanowire arrays were synthesized by electrodepositing Cu NWs in the pores of AAO templates. The sample was oxidized at 400°C for 10 h/20 h in the oxygen ambient to obtain partially oxidized CuO_x nanowires/fully oxidized CuO_x nanowires. Next, the AAO membrane was dissolved in a 1 M NaOH solution for 2 h at room temperature. The release of NWs was accelerated by sonication during the 5 s dissolution process. The NWs were then transferred and stored in pure ethanol to get a CuO_x nanowire solution.

2.4. Device Fabrication Process. For the electrical resistive switching properties measurements, typical CuO_x and Cu nanowires were drop-casted on a 200 nm thick SiO_2/Si substrate. The Ni electrodes with a thickness of 100 nm were deposited by e-beam evaporation and patterned by photolithography and lift-off processes. A typical distance between two electrodes was ~ 2 μm . Before evaporation of Ni (with a purity of 99.995% and in a vacuum at a pressure lower than 10^{-6} Torr), the sample was dipped into diluted hydrofluoric acid for 10 s to completely remove native oxide in the contact region.

2.5. Characterization. Field emission scanning electron microscopy (FE-SEM, JSM-6500F, JEOL), operating at 15 kV and field emission transmission electron microscopy (FE-TEM, JEM-3000F, JEOL) equipped with an energy dispersion spectrometer (EDS), operating at 300 kV were used to study surface morphologies and microstructures. X-ray diffraction spectrometry (Shimadzu XRD 6000, Cu $K\alpha$ radiation with a wavelength of 0.154 nm) was performed to characterize crystal structure. The resistive switching characteristics of the fabricated devices were measured by using a Keithley 4200 semiconductor parameter analyzer in atmospheric air at room temperature.

3. RESULTS AND DISCUSSION

The schematics for the fabrication procedures of CuO_x nanowire arrays are shown in Figure 1. Detailed fabrication procedures have been mentioned in the Experimental Section. Figure 2a shows a field emission scanning electron microscopy (FE-SEM) image of the fabricated AAO membrane. Note that the ~ 50 nm pore size can be confirmed. After the Cu NW growth and the oxidation process, CuO_x nanowire arrays can be achieved in pores of AAO membranes, as shown in Figure 2b. The corresponding X-ray diffraction (XRD) patterns were used to examine the phase of Cu NW arrays before and after annealing, as shown in Figure 2c. Peaks at $2\theta = 43.3^\circ$, 50.4° , and 74.08° , corresponding to (111), (200), and (220), were found, confirming the NW being of the Cu phase before annealing. After annealing as-grown Cu NW arrays at 400°C for 10 h, The diffraction peaks at $2\theta = 35.56^\circ$, 38.76° , and 66.22° indicate the ($\bar{1}11$), (111), and ($\bar{3}11$) plane orientations from the CuO phase whereas the diffraction peaks at $2\theta = 36.46^\circ$ and 42.36° indicate the (111) and (200) plane orientations from the Cu_2O phase, respectively. The results indicate that copper oxide nanowires synthesized by oxidizing the Cu nanowires consist of three phases, including, Cu, Cu_2O , and CuO, respectively.

To further shed light on oxidized phases after the oxidation process in order to discover the oxidation mechanism, a TEM image of a single NW is imperative. Figure 3a shows a low magnified TEM image of a Cu nanowire with a diameter of ~ 50 nm. Obviously, polycrystalline feature was observed for the as-grown Cu NW. The corresponding high-resolution TEM (HRTEM) image shown in Figure 3b, taken from the rectangular region in Figure 3a, clearly indicates formation of many twinned structures. The results also agree with selected area electron diffraction (SAED) pattern obtained by fast Fourier transform (FFT), as shown in inset whose (111), (200), and (220) planes belong to Cu FCC structure. The streaks along symmetric spots found in the SAED again confirm the formation of twinned structures. Figure 3c shows a TEM image of an oxidized CuO_x NW after the oxidation process. The diameter of the oxidized CuO_x nanowire still remains

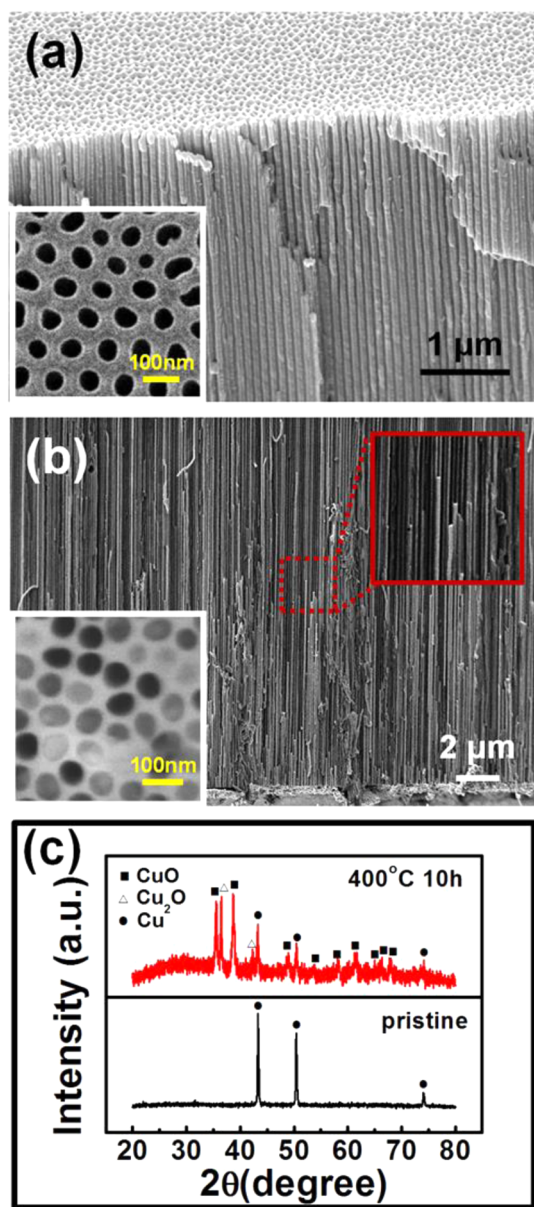


Figure 2. Cross-sectional and top view (inset) SEM images of the as-synthesized samples. (a) AAO nanotemplate with a pore diameter of ~ 50 nm and an interpore distance of ~ 100 nm. (b) Cu NW arrays embedded in AAO. (c) XRD spectra of Cu NW array in AAO before and after annealing under oxygen ambient.

unchanged due to confinement by the AAO membrane during the oxidation process. From the HRTEM image and corresponding SAED of CuO_x nanowire shown in Figure 3d, the (111) plane of Cu and Cu_2O and the (111) plane of CuO were indexed, confirming the presence of polycrystalline CuO_x phases, containing Cu, Cu_2O , and CuO phases together, which is consistent with XRD results. To further confirm the mixed phases of the CuO_x NW, electron energy loss spectrum (EELS) mapping was used. As shown in the inset of Figure 3e, the different contrasts of the O K-edge and Cu L-edge related to CuO_x nanowire were acquired. As can be seen in the EELS O K-edge image, the signal of oxygen in the outer nanowire was obviously stronger than that in the inner nanowire, revealing that the shell of the nanowire is more oxidized. In addition, nonuniform distribution oxygen in the core of the nanowire

was observed, further indicating that the NW was partially oxidized. The results were also confirmed by high angular dark field (HAADF) imaging, as shown in the inset of Figure S1 (Supporting Information) in which the image contrast is mainly determined by scattering behavior of electrons because of the different atomic mass. The larger the atomic number, the brighter the image. As a result, the darker image contrast in the outer region compared with brighter image contrast in the core region is indicative of partial oxidation of the Cu NW, which is consistent with the chemical analysis. Moreover, a distinctive difference between Cu and Cu^{2+} shown in Cu $L_{2,3}$ edge EELS spectra also provide an evidence (Figure S1, Supporting Information). Therefore, we postulate that the partially oxidized CuO_x nanowire arrays with embedded Cu nanocrystal have been synthesized by the AAO annealing method.

To investigate the intrinsic property of the CuO_x nanowire, two-terminal electric measurements on the single CuO_x NW bridged by Ni electrodes in DC voltage sweep mode were carried out by applying a voltage on one electrode while the another electrode was grounded. For comparison, the Ni/Cu NW/Ni devices were fabricated as well. All current–voltage (I – V) curves of Cu NWs and CuO_x NWs were measured in atmospheric air at room temperature. Figure 4a shows the distinctive I – V characteristics between Cu and CuO_x NWs under a small positive bias, respectively. The inset shows the corresponding SEM image of the device. The Cu NW, the resistance of which is about $\sim 40 \Omega$, exhibits a conducting linear ohmic behavior whereas the CuO_x NW shows a nonconducting characteristic. The pristine device exhibits a resistance of about $65 \text{ M}\Omega$, which is much higher than the resistance of Cu NW. As the applied bias exceeds the critical value, a dramatic drop in current is observed in Figure 4b for the Cu NW. Before that, a maximum current of $\sim 8.57 \text{ mA}$ can be measured at an applied bias of $\sim 0.66 \text{ V}$ under a sweeping rate of 10 mV per step. In our opinion, Cu NW would break down due to the thermal Joule heating effect. The corresponding SEM image is shown in the inset of Figure 4b after the nanowire breakdown. In addition, the Joule heating produced by the large current will increase the temperature of the nanowire to amplify the electron–phonon scattering when electrons transport in Cu NW^{31–33} and make Cu NW oxidized slightly, leading to a decrease of electron transport behavior in Cu NWs. The electron–phonon scattering effect and Cu oxidation explain a nonlinear behavior from I – V curves when we applied the increasing positive bias, as shown in Figure 4b. In contrast, the resistance of the CuO_x NW is relatively high and stable in the similar voltage range.

During the resistive switching measurements, a compliance current (CC) was set to protect the devices from the hard breakdown, which would result in the permanent failure. Figure 5a represents typical I – V characteristics in a Ni/ CuO_x NW/Ni device. The SEM image of corresponding device configuration is shown in the inset. When a DC voltage sweep was applied from 0 to 2.5 V with a compliance current of $10 \mu\text{A}$, a sudden increase of current was observed at $\sim 1.375 \text{ V}$. The resistance changes from pristine resistance state to low-resistance state (LRS or ON-state), defined as the “SET” process, and the corresponding applied voltage is called SET voltage (V_{SET}). Subsequently, when the voltage bias was swept from 0 to -1 V , the resistance of the device transited back to high-resistance state (HRS or OFF-state), which is called the “RESET process” and the corresponding voltage, is called RESET voltage (V_{RESET}). This kind of resistive switching whose SET/RESET voltages having an opposite polarity is called bipolar switching.

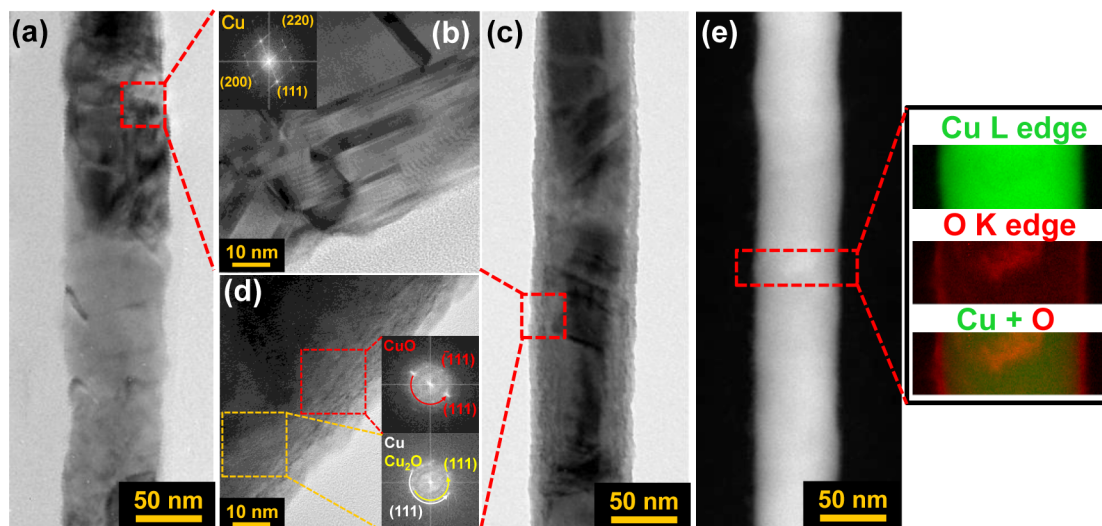


Figure 3. TEM analyses of Cu and CuO_x NW. (a) Bright field image of a typical Cu NW. (b) High resolution TEM image of Cu NW. Inset shows the corresponding selected area diffraction pattern obtained by FFT process. (c) Bright field image of a CuO_x NW. (d) High resolution TEM image of a CuO_x NW. Inset shows the corresponding selected area diffraction patterns obtained by FFT process. (e) HAADF image of a CuO_x NW. Inset shows the EELS mapping images at Cu L-edge and O K-edge from the selected region.

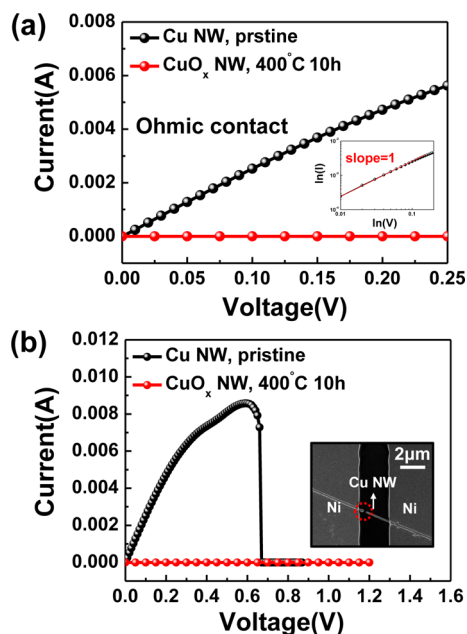


Figure 4. Electrical I - V characteristics of Cu NW and CuO_x NW. (a) Distinctive metallic behavior can be found. Inset shows a typical Ohmic behavior in logarithm scale. (b) Dramatic current drop occurs to Cu NW NW once the bias was applied over 0.6 V whereas no current change to CuO_x occurs at applied bias <1.2 V.

In addition, Figure 5b shows unipolar switching of the CuO_x NW devices. The results indicate that the CuO_x NW devices actually exhibit a nonpolar switching behavior in the symmetric MIM configuration. However, the unipolar switching is not stable (Figure S2, Supporting Information) and reversible switching can be observed only when the devices are operated in bipolar mode. More typical bipolar switching I - V curves are shown in Figure S3 (Supporting Information). It is clearly seen that the threshold voltages of SET and RESET are relatively small (~ 1 V) in either switching mode. Besides, the requirement of forming process to activate resistive switching operation is one of the critical issues for ReRAM practical

application. It is quite interesting that the CuO_x NW could trigger a resistive switch effect without a “forming process”. Note that the $V_{\text{SET}} = 1.375$ V with an electric field of about ~ 6.8 kV/cm is relatively small, having the potential to reduce the power consumption. For comparison, Table 1 tabulates the performance of devices in this work and the presents copper oxide-based resistive switching memories reported in the previous literature. In general, threshold voltage is proportional to film thickness/distance between the two electrodes. The threshold electric field in CuO_x nanowire device is much smaller than those of thin films cases. Furthermore, the operation with the small bias and forming-free property of the polycrystalline CuO_x nanowire is attractive when compared with the other single crystalline nanowire-based memristor works.^{19–21,24,32} In addition, the fully oxidized nanowires were synthesized by extending the annealing time (20 h of annealing), where the originally smooth surface of the nanowire was converted to the rough one shown in Figure S1. It is because of the different volume change during formation of many small aggregated CuO_x grains. The corresponding SAED of the fully oxidized CuO_x nanowire is shown in Figure S2, for which the (111) plane of CuO was indexed. Cavity regions were clearly observed in the HAADF image (Figure S3), which is most likely owing to the volume change of the phase transformation from Cu to CuO_x .³³ The current–voltage (I - V) characteristics of fully oxidized CuO_x nanowires are shown in Figure S3. It is noted that the device did not exhibit a resistive switching behavior even when the bias was applied up to 40 V. That is, the resistive switching properties only occur in the partially oxidized CuO_x nanowires. Figure S4 shows the double-logarithmic I - V plot of the Ni/ CuO_x NW/Ni devices. Obviously, a linear proportion at HRS from the log I - V plot indicates an Ohmic conduction behavior ($I \propto V$) at a low voltage region (<1 V) and gradually changes to the Child’s law region,³⁴ for which the current is proportional to the square of the voltage ($I \propto V^2$). This behavior is qualitatively interpreted to follow the shallow trap-associated space charge limited current (SCLC) theory with an equation of $I(V) = aV + bV^2$.³⁴

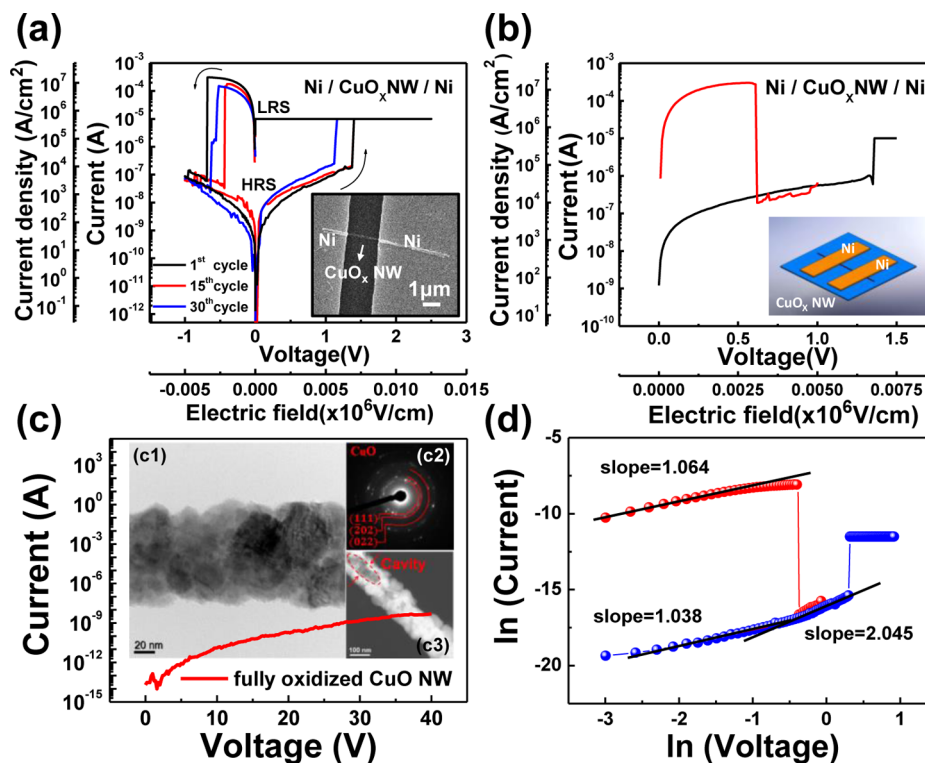


Figure 5. (a) Typical bipolar resistive switching $I-V$ characteristic of Ni/CuO_x NW/Ni device in logarithm scale. Inset shows a SEM image of a Ni/CuO_x NW/Ni device. The distance between two electrodes of $\sim 2 \mu m$ can be found. (b) Typical unipolar resistive switching $I-V$ characteristics of Ni/CuO_x NW/Ni devices in logarithm scale. Inset shows a schematic of a Ni/CuO_x NW/Ni device. (c) Electrical $I-V$ characteristics of fully oxidized CuO NW. (c1) Bright field TEM image shows the rough surface. (c2) Corresponding SAED pattern. (c3) Dark field TEM image reveals the existence of the cavity. (d) Corresponding double-logarithmic $I-V$ curves.

Table 1. Summary of Copper Oxide based Resistive Switching Memories

device structure	thickness (electrode distance)	V_{set} (V)	E_{set} (MV/cm)	ref
Cu/Cu ₂ O/Ni	6–8 nm	1.6	2.29	9
Cu/Cu ₂ O/Ti	12 nm	2.7	2.25	40
Cu/Cu ₂ O/Ni	12 nm	3.3	2.75	41
TiN/CuO _x /Pt	70 nm	0.83	0.12	42
Cu/CuO/Al	250 nm	2.7	0.108	43
Pt/CuO/Au	300 nm	3.7	0.123	44
Pt/Cu ₂ O/Pt	190 nm	2.6	0.137	45
Pt/CuO/Pt	2.1 μm	12	5.71×10^{-2}	46
Ni/CuO _x	2 μm	1.35	6.75×10^{-3}	this work
NW/Ni				

In general, pristine-state oxide materials are too insulative to induce reliable resistive switching due to the low density of defects such as oxygen vacancies or metal interstitials.^{35,36} Therefore, an electroforming process is a prerequisite to operate a device, which is an obstacle for ReRAM commercial applications. In the case of the present work, there is a significant amount of oxygen vacancies (V_O) in CuO_x NW due to the coexistence of Cu₂O/CuO and Cu nanograins, which triggers a low electric-field-induced switching operation with the forming free behavior, as shown in Figure 6a. During the SET process, as shown in Figure 6b, oxygen vacancies diffuse from the anode (the electrode on which the voltage was

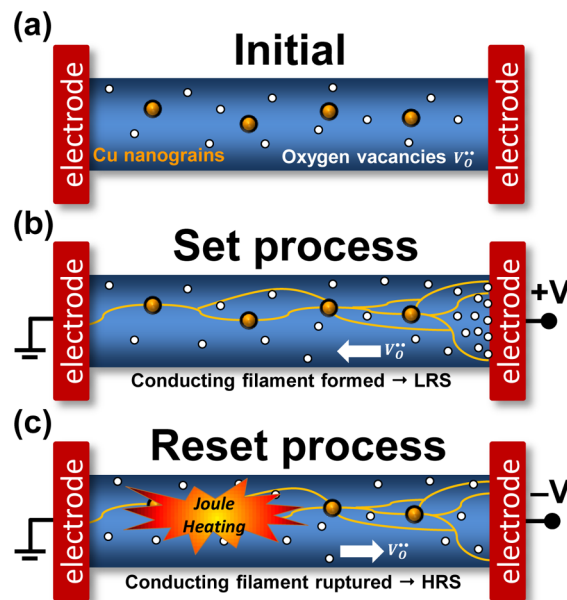


Figure 6. Schematics of resistive switching mechanism. (a) Initial state before set process, (b) set process, and (c) reset process.

applied) to cathode (grounded electrode) and form metallic filaments under the electric field. Extra oxygen vacancies can be generated at the interface between CuO_x NW and anode. Simultaneously, electrons are injected from cathode to anode. The Joule heating effect by electron injection should provide a thermal energy to drive ionic migration. The metallic Cu

components, as nanoparticles embedded in the CuO_x nanowire, enhance the diffusion of mobile oxygen vacancies and induce local electric field enhancement.^{37,38} In addition, the geometry of a confined nanowire configuration offers a large area surface and a direct moving path for diffusion of oxygen vacancies to induce the stable switching. In the RESET process, a significant amount of heat generated by the Joule heating interrupts the local filaments and the conducting paths of electron are broken when high current density flows into the metallic filaments (Figure 6c). Simultaneously, Joule heating also provides energy to the thermochemical reaction, causing the migration of oxygen vacancies (oxygen ions). Notice that positions for the rupture of the filaments would normally occur near the grounded electrode because of much finer filament sizes.³⁹ As a result, both Joule heating and electric field play an important role in resistive switching, simultaneously.^{4,35} However, the interruption of the conducting filaments is mainly due to the Joule heating in the nonpolar device.^{4,35,36} Yet, the migration of oxygen vacancies under the positive bias results in the formation or the reconstruction of the conducting filaments. Different stabilities of resistive switching between unipolar and bipolar mode are observed. When the devices are manipulated in the unipolar mode, oxygen vacancies would consecutively drift to the cathode under the positive bias. As a result, it is likely that conducting filaments would be formed again right after the Joule heating takes place (Figure S2b, Supporting Information). On the other hand, the diffusion of oxygen vacancies by an electric field would localize the formation and rupture of conducting filaments near the grounded electrode when the devices are manipulated in bipolar mode.^{35,36} Therefore, the migration of oxygen vacancies also enhances the switching stability.

Figure 7a shows the switching endurance tests of nanowire devices. Obtained by repetitive ON/OFF sweeping operation, the endurance cycling test could reach to 50 times. The memory window is defined by the two resistance states as $(R_{\text{OFF}} - R_{\text{ON}})/R_{\text{ON}} \approx R_{\text{OFF}}/R_{\text{ON}}$. The typical resistances of the

ON-state are an order of $10^3 \Omega$ and those of the OFF-state are on the order of $10^6 \sim 10^9 \Omega$, showing that the memory window is more than 10^3 . Statistical results of HRS and LRS in the different nanowire devices are shown in Figure S4 (Supporting Information). The larger the memory window, the less chance for misreading of the resistance states, and it also has the potential for high density multistate memory application by using different compliance currents.³⁹ The dynamic responses of CuO_x NW devices were also performed, as shown in Figure S5 (Supporting Information), showing the potential for real applications during the consecutive pulse measurements. Clearly, ON/OFF ratios are still 3 orders of magnitude compared with DC sweep endurance data. Furthermore, we have applied a smaller pulse ($50 \mu\text{s}$) to devices but none of them show the resistive switching due to the micrometer scale ($\sim 2 \mu\text{m}$) channel length of our devices. We postulate that a quicker response of devices can be expected at a smaller channel length. Figure 7b shows cumulative probability distributions of SET and RESET voltages (V_{SET} and V_{RESET}) for different switching cycles performed on the Ni/ CuO_x NW/Ni device. The V_{SET} and V_{RESET} distribute in the ranges of 0.875 to 2.25 V and -0.43 to -0.78 V, respectively. The variation of V_{RESET} is much more narrower than that of V_{SET} , which is evidence that conducting filaments play a dominant role in resistive switching characteristics in a single CuO_x NW. Judging from the filamentary resistive switching mechanism, the formation of conducting filament in the SET process should be more random than the rupture of an existing filament during the RESET process.³⁵ Therefore, the formation process is determined by the competition among different filamentary paths with variable locations, random orientations, and uncertain sizes of conducting filaments.⁸ Because the RESET process is caused by the Joule heating effect to burn out the existing filament paths, a larger distribution in V_{SET} should be expected. The switching cycle performance is still limited by the breakdown of the nanowire owing to the Joule heating effect, which is expected to be improved in our following work. However, the resistive switching property could be operated in a single CuO_x NW ~ 50 nm in diameter. In other words, it confirms that the ReRAM device could be scaled down to the 50 nm region.

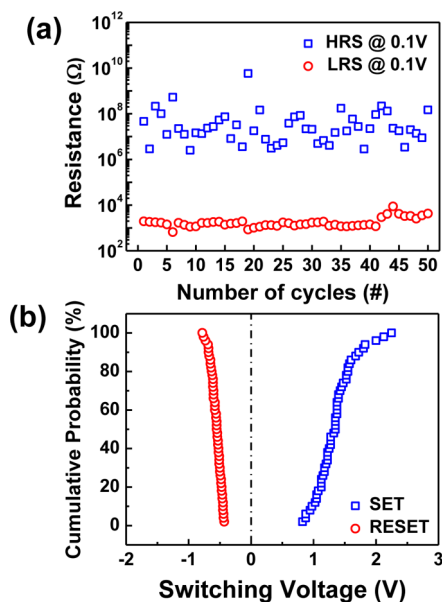


Figure 7. (a) Endurance test of the Ni/ CuO_x NW/Ni device under DC voltage sweep mode at read voltage of 0.1 V. (b) Cumulative distribution plot of V_{SET} and V_{RESET} for the Ni/ CuO_x NW/Ni device.

4. CONCLUSIONS

In summary, the resistive switching effect in CuO_x NW synthesized by a low-cost and large-scale electrochemical process with AAO nanotemplates at low temperatures was successfully demonstrated. The CuO_x NW memory devices exhibit a forming-free property, low electric-field-induced switching operation because of a significant amount of defects and Cu nanocrystals in the CuO_x nanowires. Detailed resistive switching mechanisms are systematically proposed and investigated. This work is expected to have not only the opportunity to help in the exploration of forming-free resistive switching mechanisms but also the potential to improve performance for resistive memory devices.

■ ASSOCIATED CONTENT

Supporting Information

EELS Cu $L_{2,3}$ edge spectra of the CuO_x NW; unipolar operation of CuO_x NW; device yield; statistical results of HRS and LRS, switching endurance data of the CuO_x NW device. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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Notes

The authors declare no competing financial interest.

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